Chapter 4
DC Biasing — BJTs

Chapter Outline

4.1 Introduction

The analysis or design of a transistor amplifier requires a knowledge of both the dc and the ac response of the system. Too often it is assumed that the transistor is a magical device that can raise the level of the applied ac input without the assistance of an external energy source. In actuality,

the improved output ac power level is the result of a transfer of energy from the applied dc supplies.

The analysis or design of any electronic amplifier therefore has two components: the dc portion and the ac portion. Fortunately, the superposition theorem is applicable and the investigation of the dc conditions can be totally separated from the ac response. However, one must keep in mind that during the design or synthesis stage the choice of parameters for the required dc levels will affect the ac response, and vice versa.

The dc level of operation of a transistor is controlled by a number of factors, including the range of possible operating points on the device characteristics. In Section 4.2 we specify the range for the bipolar junction transistor (BJT) amplifier. Once the desired dc current and voltage levels have been defined, a network must be constructed that will establish the desired operating point. A number of these networks are analyzed in this chapter. Each design will also determine the stability of the system, that is, how sensitive the system is to temperature variations, another topic to be investigated in a later section of this chapter.

Although a number of networks are analyzed in this chapter, there is an underlying similarity in the analysis of each configuration due to the recurring use of the following important basic relationships for a transistor:

$$\boxed{V_{BE} = 0.7\ \text{V}} \tag{4.1}$$

$$\boxed{I_E = (\beta + 1)I_B \cong I_C} \tag{4.2}$$

$$\boxed{I_C = \beta I_B} \tag{4.3}$$

In fact, once the analysis of the first few networks is clearly understood, the path toward the solution of the networks to follow will begin to become quite apparent. In most instances the base current I_B is the first quantity to be determined. Once I_B is known, the relationships of Eqs. (4.1) through (4.3) can be applied to find the remaining quantities of interest. The similarities in analysis will be immediately obvious as we progress through the chapter. The equations for I_B are so similar for a number of configurations that one equation can be derived from another simply by dropping or adding a term or two. The primary function of this chapter is to develop a level of familiarity with the BJT transistor that would permit a dc analysis of any system that might employ the BJT amplifier.

4.2 Operating Point

The term *biasing* appearing in the title of this chapter is an all-inclusive term for the application of dc voltages to establish a fixed level of current and voltage. For transistor amplifiers the resulting dc current and voltage establish an *operating point* on the characteristics that define the region that will be employed for amplification of the applied signal. Since the operating point is a fixed point on the characteristics, it is also called the *quiescent point* (abbreviated *Q*-point). By definition, *quiescent* means quiet, still, inactive. Fig. 4.1 shows a general output device characteristic with four operating points indicated. The biasing circuit can be designed to set the device operation at any of these points or others within the *active region*. The maximum ratings are indicated on the characteristics of Fig. 4.1 by a horizontal line for the maximum collector current $I_{C_{\max}}$ and a vertical line at the maximum collector-to-emitter voltage $V_{CE_{\max}}$. The maximum power constraint is defined by the curve $P_{C_{\max}}$ in the same figure. At the lower end of the scales are the *cutoff region*, defined by $I_B \leq 0$ μA, and the *saturation region*, defined by $V_{CE} \leq V_{CE_{\text{sat}}}$.

The BJT device could be biased to operate outside these maximum limits, but the result of such operation would be either a considerable shortening of the lifetime of the device or destruction of the device. Confining ourselves to the *active* region, we can select many different operating areas or points. The chosen *Q*-point often depends on the intended use of the circuit. Still, we can consider some differences among the various points shown in Fig. 4.1 to present some basic ideas about the operating point and, thereby, the bias circuit.

If no bias were used, the device would initially be completely off, resulting in a *Q*-point at *A* — namely, zero current through the device (and zero voltage across it). Since it is necessary to bias a device so that it can respond to the entire range of an input signal, point *A* would not be suitable. For point *B*, if a signal is applied to the circuit, the device will vary in current and voltage from the operating point, allowing the device to react to (and possibly amplify) both the positive and negative excursions of the input signal. If the input signal is properly chosen, the voltage and current of the device will vary but not enough to drive the device into *cutoff* or *saturation*. Point *C* would allow some positive and negative variation of the output signal, but the peak-to-peak value would be limited by the proximity of $V_{CE} = 0$ V and $I_C = 0$ mA. Operating at point *C* also raises some concern about the nonlinearities intro-

duced by the fact that the spacing between I_B curves is rapidly changing in this region. In general, it is preferable to operate where the gain of the device is fairly constant (or linear) to ensure that the amplification over the entire swing of input signal is the same. Point *B* is a region of more linear spacing and therefore more linear operation, as shown in Fig. 4.1. Point *D* sets the device operating point near the maximum voltage and power level. The output voltage swing in the positive direction is thus limited if the maximum voltage is not to be exceeded. Point *B* therefore seems the best operating point in terms of linear gain and largest possible voltage and current swing. This is usually the desired condition for small-signal amplifiers (Chapter 5) but not the case necessarily for power amplifiers, which will be considered in Chapter 11. In this discussion, we will be concentrating primarily on biasing the transistor for *small-signal* amplification operation.

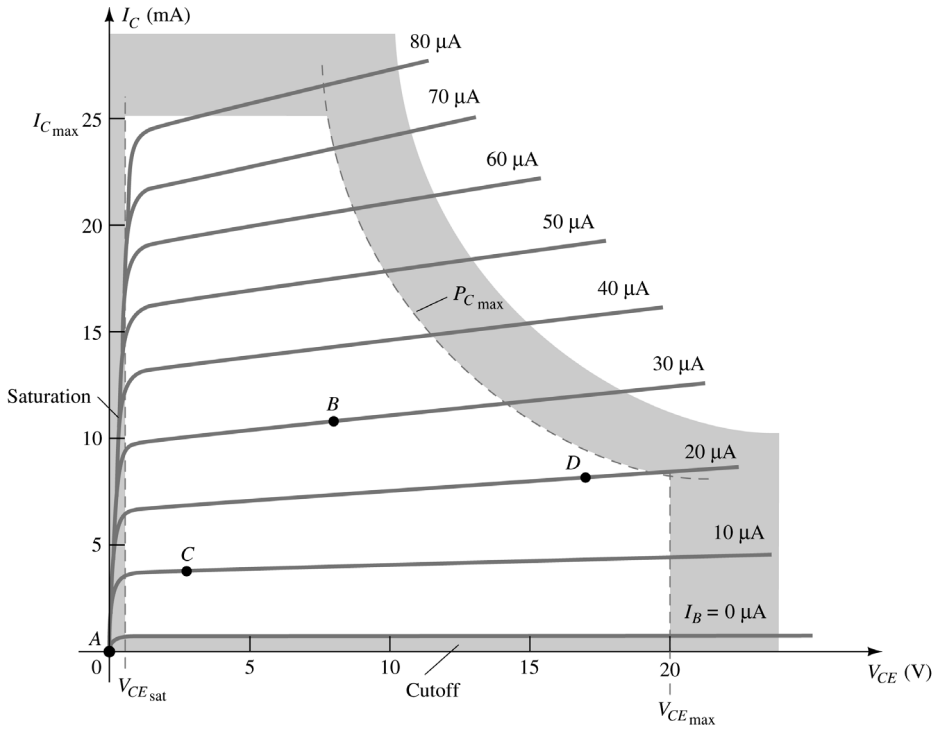

Fig. 4.1 Various operating points within the limits of operation of a transistor.

One other very important biasing factor must be considered. Having selected and biased the BJT at a desired operating point, we must also take the effect of temperature into account. Temperature causes the device parameters such as the transistor current gain (β_{ac}) and the transistor leakage current (I_{CEO}) to change. Higher temperatures result in increased leakage currents in the device, thereby changing the operating condition set by the biasing network. The result is that the network design must also provide a degree of *temperature stability* so that temperature changes result in minimum changes in the operating point. This maintenance of the operating point can be specified by a *stability factor S*, which indicates the degree of change in operating point due to a temperature variation. A highly stable circuit is desirable, and the stability of a few basic bias circuits will be compared.

For the BJT to be biased in its linear or active operating region the following must be true:

1. *The base-emitter junction* must *be forward-biased (*p-*region voltage more* p*ositive), with a resulting forward-bias voltage of about 0.6 to 0.7 V.*
2. *The base-collector junction* must *be reverse-biased (*n-*region more* p*ositive), with the reverse-bias voltage being any value within the maximum limits of the device.*

[Note that for forward bias the voltage across the *p-n* junction is *p-p*ositive, whereas for reverse bias it is opposite (reverse) with *n*-positive. This emphasis on the initial letter should provide a means of helping memorize the necessary voltage polarity.]

Operation in the cutoff, saturation, and linear regions of the BJT characteristic are provided as follows:

1. *Linear-region operation:*
   Base-emitter junction forward-biased
   Base-collector junction reverse-biased
2. *Cutoff-region operation:*
   Base-emitter junction reverse-biased
   Base-collector junction reverse-biased
3. *Saturation-region operation:*
   Base-emitter junction forward-biased
   Base-collector junction forward-biased

4.3 Fixed-Bias Circuit

The fixed-bias circuit of Fig. 4.2 is the simplest transistor dc bias configuration. Even though the network employs an *npn* transistor, the equations and calculations apply equally well to a *pnp* transistor configuration merely by changing all current directions and voltage polarities. The current directions of Fig. 4.2 are the *actual* current directions, and the voltages are defined by the standard double-subscript notation. For the dc analysis the network can be isolated from the indicated ac levels by replacing the capacitors with an open-circuit equivalent because the reactance of a capacitor for dc is $X_C = 1/2\pi fC = 1/2\pi(0)C = \infty\ \Omega$. In addition, the dc supply V_{CC} can be separated into two supplies (for analysis purposes only) as shown in Fig. 4.3 to permit a separation of input and output circuits. It also reduces the linkage between the two to the base current I_B. The separation is certainly valid, as we note in Fig. 4.3 that V_{CC} is connected directly to R_B and R_C just as in Fig. 4.2.

Forward Bias of Base-Emitter

Consider first the base-emitter circuit loop of Fig. 4.4. Writing Kirchhoff's voltage equation in the clockwise direction for the loop, we obtain

$$+V_{CC} - I_B R_B - V_{BE} = 0$$

Note the polarity of the voltage drop across R_B as established by the indicated direction of I_B. Solving the equation for the current I_B results in the following:

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B}} \tag{4.4}$$

Equation (4.4) is certainly not a difficult one to remember if one simply keeps in mind that the base current is the current through R_B and by Ohm's law that current is the voltage across R_B divided by the resistance R_B. The voltage across R_B is the applied voltage V_{CC} at one end less the drop across the base-to-emitter junction (V_{BE}). In addition, since the supply voltage V_{CC} and the base-emitter voltage V_{BE} are constants, the selection of a base resistor R_B sets the level of base current for the operating point.

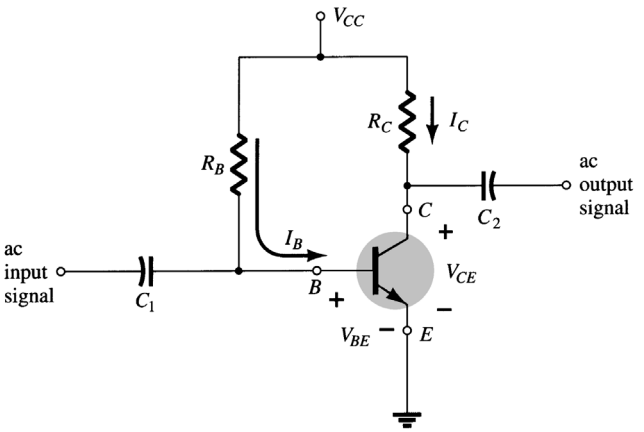

Fig. 4.2 Fixed-bias circuit.

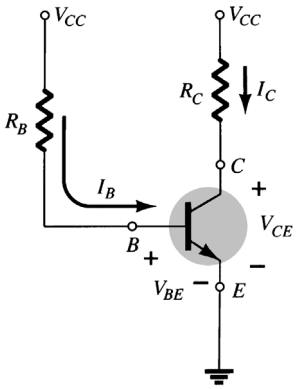

Fig. 4.3 DC equivalent of Fig. 4.2.

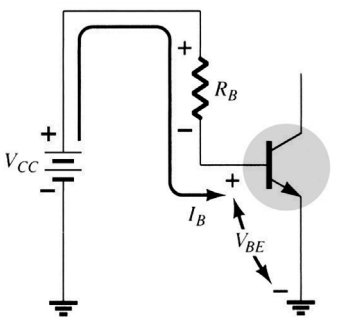

Fig. 4.4 Base–emitter loop.

Collector-emitter Loop

The collector-emitter section of the network appears in Fig. 4.5 with the indicated direction of current I_C and the resulting polarity across R_C. The magnitude of the collector current is related directly to I_B through

$$I_C = \beta I_B \tag{4.5}$$

It is interesting to note that since the base current is controlled by the level of R_B and I_C is related to I_B by a constant β, the magnitude of I_C is not a function of the resistance R_C. Changing R_C to any level will not affect the level of I_B or I_C as long as we remain in the active region of the device. However, as we shall see, the level of R_C will determine the magnitude of V_{CE}, which is an important parameter.

Applying Kirchhoff's voltage law in the clockwise direction around the indicated closed loop of Fig. 4.5 results in the following:

$$V_{CE} + I_C R_C - V_{CC} = 0$$

and

$$\boxed{V_{CE} = V_{CC} - I_C R_C} \tag{4.6}$$

which states that the voltage across the collector-emitter region of a transistor in the fixed-bias configuration is the supply voltage less the drop across R_C.

As a brief review of single- and double-subscript notation recall that

$$\boxed{V_{CE} = V_C - V_E} \tag{4.7}$$

where V_{CE} is the voltage from collector to emitter and V_C and V_E are the voltages from collector and emitter to ground, respectively. *In this case*, since $V_E = 0$ V, we have

$$\boxed{V_{CE} = V_C} \tag{4.8}$$

In addition, since

$$\boxed{V_{BE} = V_B - V_E} \tag{4.9}$$

and $V_E = 0$ V, then

$$\boxed{V_{BE} = V_B} \tag{4.10}$$

Keep in mind that voltage levels such as V_{CE} are determined by placing the red (positive) lead of the voltmeter at the collector terminal with the black (negative) lead at the emitter terminal as shown in Fig. 4.6. V_C is the voltage from collector to ground and is measured as shown in the same figure. In this case the two readings are identical, but in the networks to follow the two can be quite different. Clearly understanding the difference between the two measurements can prove to be quite important in the troubleshooting of transistor networks.

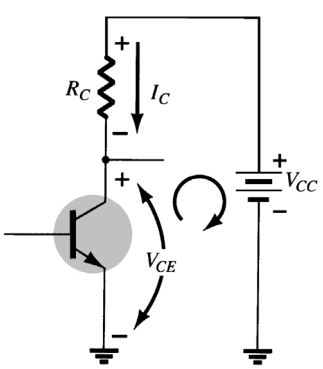

Fig. 4.5 Collector–emitter loop.

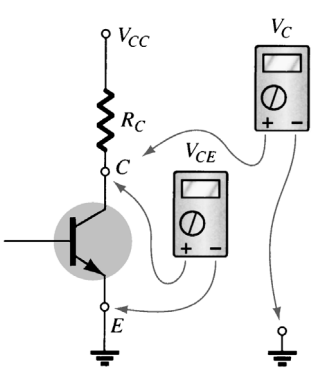

Fig. 4.6 Measuring V_{CE} and V_C.

Example 4.1 Determine the following for the fixed-bias configuration of Fig. 4.7.

a. I_{B_Q} and I_{C_Q}.

b. V_{CE_Q}.

c. V_B and V_C.

d. V_{BC}.

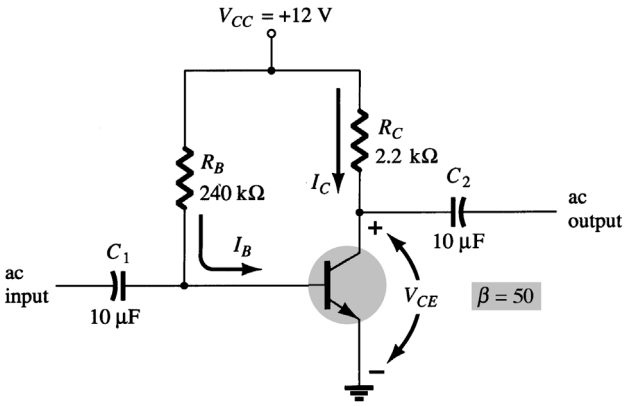

Fig. 4.7 DC fixed-bias circuit for Example 4.1.

Solution:

a. Eq. (4.4): $$I_{B_Q} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\text{ V} - 0.7\text{ V}}{240\text{ k}\Omega} = \mathbf{47.08\ \mu A}$$

Eq. (4.5): $$I_{C_Q} = \beta I_{B_Q} = (50)(47.08\ \mu\text{A}) = \mathbf{2.35\ mA}$$

b. Eq. (4.6): $$V_{CE_Q} = V_{CC} - I_C R_C$$
$$= 12\text{ V} - (2.35\text{ mA})(2.2\text{ k}\Omega)$$
$$= \mathbf{6.83\ V}$$

c. $V_B = V_{BE} = \mathbf{0.7\ V}$

$V_C = V_{CE} = \mathbf{6.83\ V}$

d. Using double-subscript notation yields

$$V_{BC} = V_B - V_C = 0.7\text{ V} - 6.83\text{ V}$$
$$= \mathbf{-6.13\ V}$$

with the negative sign revealing that the junction is reversed-biased, as it should be for linear amplification.

Transistor Saturation

The term *saturation* is applied to any system where levels have reached their maximum values. A saturated sponge is one that cannot hold another drop of liquid. For a transistor operating in the saturation region, the current is a maximum value *for the particular design*. Change the design and the corresponding saturation level may rise or drop. Of course, the highest saturation level is defined by the maximum collector current as provided by the specification sheet.

Saturation conditions are normally avoided because the base-collector junction is no longer reverse-biased and the output amplified signal will be distorted. An operating point in the saturation

region is depicted in Fig. 4.8a. Note that it is in a region where the characteristic curves join and the collector-to-emitter voltage is at or below $V_{CE_{sat}}$. In addition, the collector current is relatively high on the characteristics.

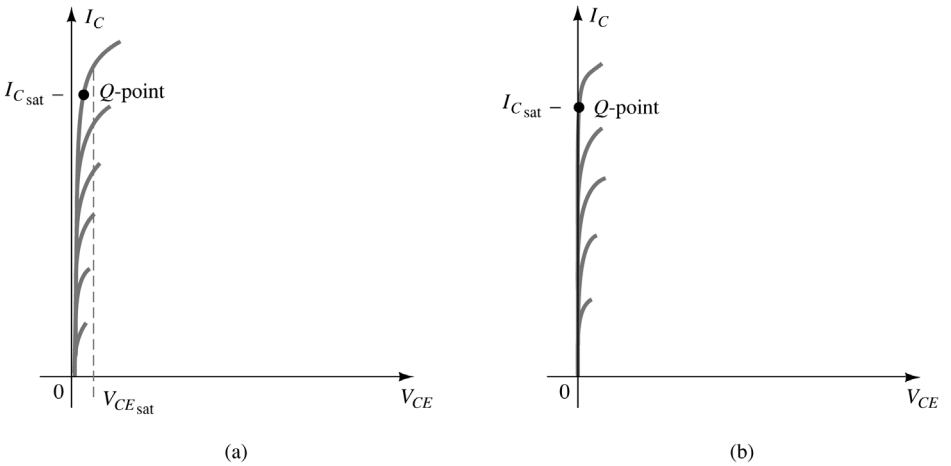

Fig. 4.8 Saturation regions: (a) actual; (b) approximate.

If we approximate the curves of Fig. 4.8a by those appearing in Fig. 4.8b, a quick, direct method for determining the saturation level becomes apparent. In Fig. 4.8b, the current is relatively high and the voltage V_{CE} is assumed to be 0 V. Applying Ohm's law, we can determine the resistance between collector and emitter terminals as follows:

$$R_{CE} = \frac{V_{CE}}{I_C} = \frac{0\text{ V}}{I_{C_{sat}}} = 0\ \Omega$$

Applying the results to the network schematic results in the configuration of Fig. 4.9.

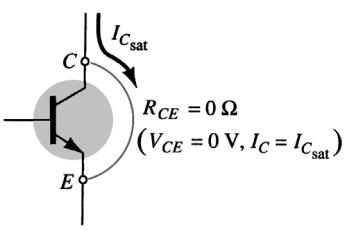

Fig. 4.9 Determining $I_{C_{sat}}$.

For the future, therefore, if there were an immediate need to know the approximate maximum collector current (saturation level) for a particular design, simply insert a short-circuit equivalent between collector and emitter of the transistor and calculate the resulting collector current. In short, set $V_{CE} = 0$ V. For the fixed-bias configuration of Fig. 4.10, the short circuit has been applied, causing the voltage across R_C to be the applied voltage V_{CC}. The resulting saturation current for the fixed-bias configuration is

$$I_{C_{sat}} = \frac{V_{CC}}{R_C} \tag{4.11}$$

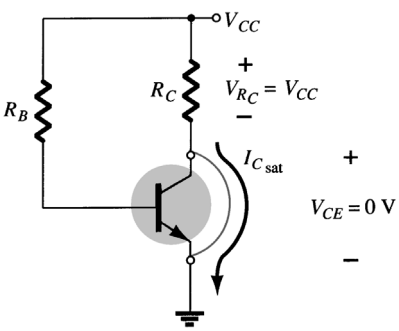

Fig. 4.10 Determining $I_{C_{sat}}$ for the fixed-bias configuration.

Once $I_{C_{sat}}$ is known, we have some idea of the maximum possible collector current for the chosen design and the level to stay below if we expect linear amplification.

Example 4.2 Determine the saturation level for the network of Fig. 4.7.

Solution:

$$I_{C_{sat}} = \frac{V_{CC}}{R_C} = \frac{12\text{ V}}{2.2\text{ k}\Omega} = \mathbf{5.45\text{ mA}}$$

The design of Example 4.1 resulted in $I_{C_Q} = 2.35$ mA. which is far from the saturation level and about one-half the maximum value for the design.

Load-Line Analysis

The analysis thus far has been performed using a level of β corresponding to the resulting Q-point. We will now investigate how the network parameters define the possible range of Q-points and how the actual Q-point is determined. The network of Fig. 4.11a establishes an output equation that relates the variables I_C and V_{CE} in the following manner:

$$V_{CE} = V_{CC} - I_C R_C \tag{4.12}$$

The output characteristics of the transistor also relate the same two variables I_C and V_{CE} as shown in Fig. 4.11b.

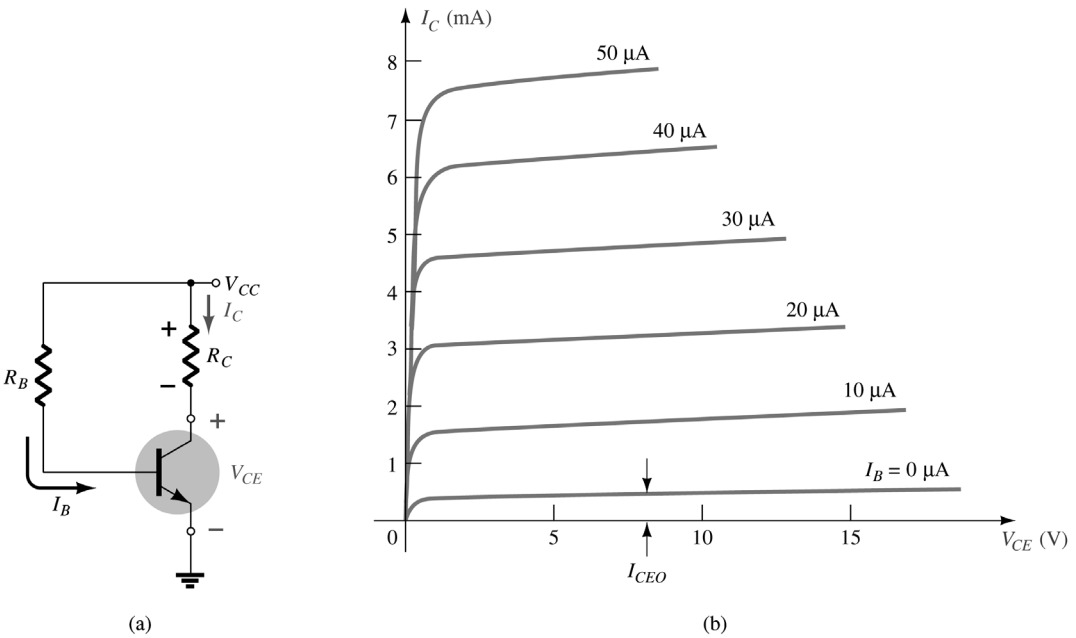

Fig. 4.11 Load-line analysis: (a) the network; (b) the device characteristics.

In essence, therefore, we have a network equation and a set of characteristics that employ the same variables. The common solution of the two occurs where the constraints established by each are satisfied simultaneously. In other words, this is similar to finding the solution of two simultaneous equations: one established by the network and the other by the device characteristics.

The device characteristics of I_C versus V_{CE} are provided in Fig. 4.11b. We must now superimpose the straight line defined by Eq. (4.12) on the characteristics. The most direct method of plotting Eq. (4.12) on the output characteristics is to use the fact that a straight line is defined by two points. If we *choose* I_C to be 0 mA, we are specifying the horizontal axis as the line on which one point is located. By substituting $I_C = 0$ mA into Eq. (4.12), we find that

$$V_{CE} = V_{CC} - (0)R_C$$

and

$$\boxed{V_{CE} = V_{CC}\big|_{I_C=0\text{ mA}}} \tag{4.13}$$

defining one point for the straight line as shown in Fig. 4.12.

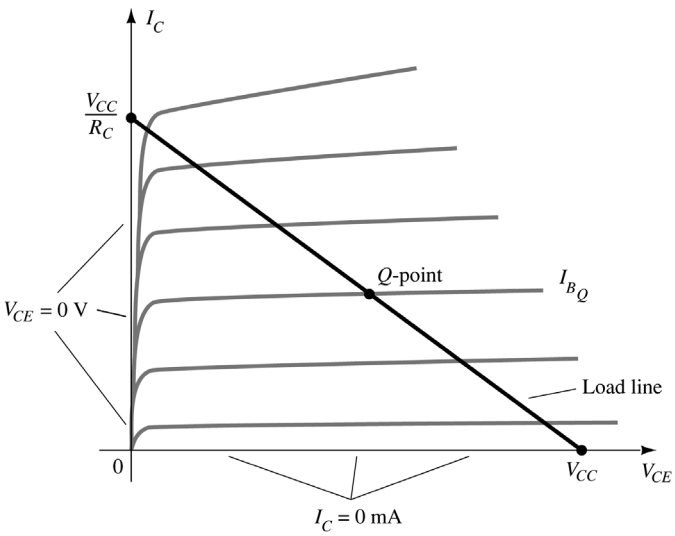

Fig. 4.12 Fixed-bias load line.

If we now *choose* V_{CE} to be 0 V, which establishes the vertical axis as the line on which the second point will be defined, we find that I_C is determined by the following equation:

$$0 = V_{CC} - I_C R_C$$

and

$$\boxed{I_C = \frac{V_{CC}}{R_C}\bigg|_{V_{CE}=0\text{ V}}} \tag{4.14}$$

as appearing on Fig. 4.12.

By joining the two points defined by Eqs. (4.13) and (4.14), we can draw the straight line established by Eq. (4.12). The resulting line on the graph of Fig. 4.12 is called the *load line* since it is defined by the load resistor R_C. By solving for the resulting level of I_B, we can establish the actual Q-point as shown in Fig. 4.12.

If the level of I_B is changed by varying the value of R_B, the Q-point moves up or down the load line as shown in Fig. 4.13. If V_{CC} is held fixed and R_C changed, the load line will shift as shown in Fig. 4.14. If I_B is held fixed, the Q-point will move as shown in the same figure. If R_C is fixed and V_{CC} varied, the load line shifts as shown in Fig. 4.15.

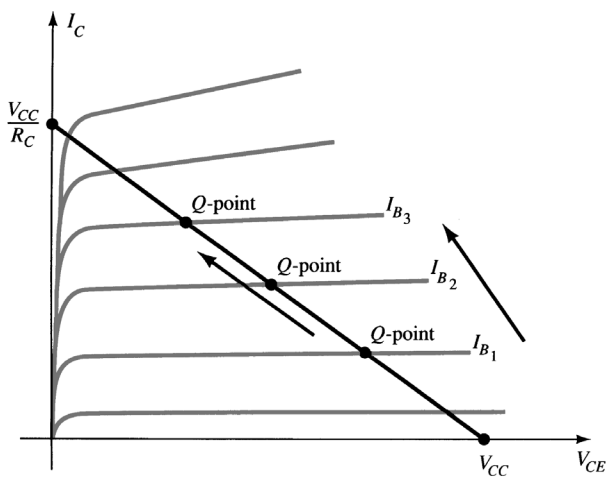

Fig. 4.13 Movement of the *Q*-point with increasing level of I_B.

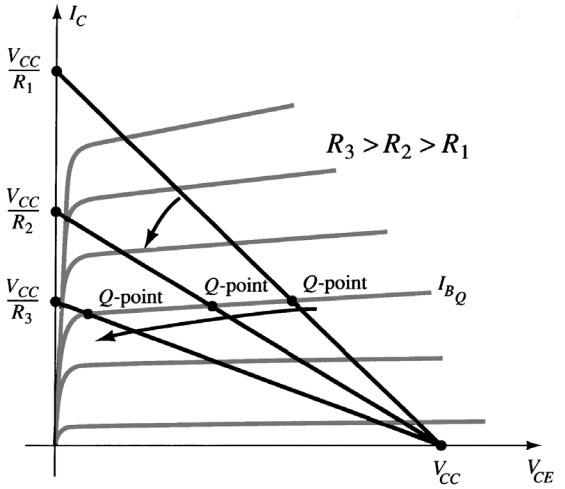

Fig. 4.14 Effect of an increasing level of R_C on the load line and the *Q*-point.

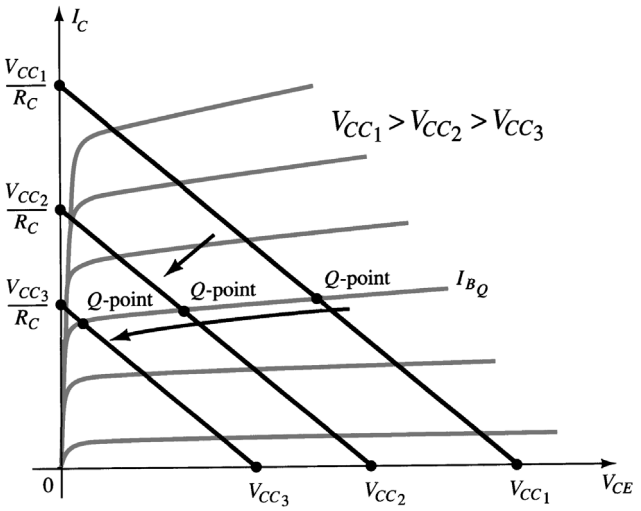

Fig. 4.15 Effect of lower values of V_{CC} on the load line and the *Q*-point.

Example 4.3 Given the load line of Fig. 4.16 and the defined *Q*-point, determine the required values of V_{CC}, R_C, and R_B for a fixed-bias configuration.

Solution: From Fig. 4.16,

$$V_{CE} = V_{CC} = \mathbf{20\ V} \text{ at } I_C = 0\,\text{mA}$$

$$I_C = \frac{V_{CC}}{R_C} \text{ at } V_{CE} = 0\,\text{V}$$

and

$$R_C = \frac{V_{CC}}{I_C} = \frac{20\text{ V}}{10\text{ mA}} = \mathbf{2\ k\Omega}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

and

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{20\text{ V} - 0.7\text{ V}}{25\ \mu\text{A}} = \mathbf{772\ k\Omega}$$

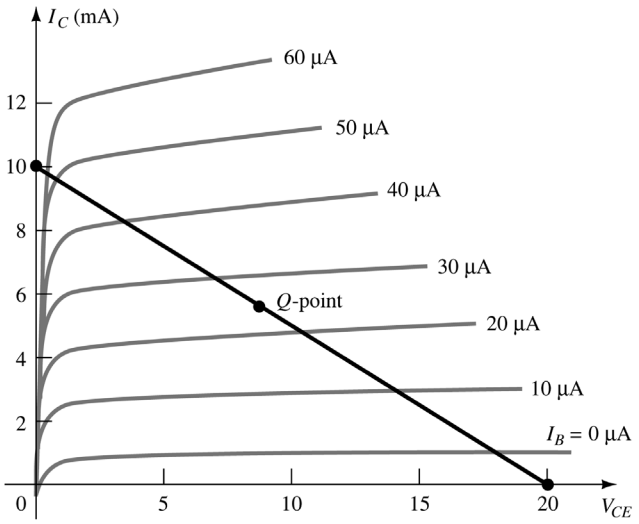

Fig. 4.16 Example 4.3.

4.4 Emitter Bias

The dc bias network of Fig. 4.17 contains an emitter resistor to improve the stability level over that of the fixed-bias configuration. The improved stability will be demonstrated through a numerical example later in the section. The analysis will be performed by first examining the base-emitter loop and then using the results to investigate the collector-emitter loop.

Base-Emitter Loop

The base-emitter loop of the network of Fig. 4.17 can be redrawn as shown in Fig. 4.18. Writing Kirchhoff's voltage law around the indicated loop in the clockwise direction results in the following equation:

$$+V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0 \tag{4.15}$$

Recall from Chapter 3 that

$$I_E = (\beta + 1) I_B \tag{4.16}$$

Substituting for I_E in Eq. (4.15) results in

$$V_{CC} - I_B R_B - V_{BE} - (\beta + I) I_B R_E = 0$$

Grouping terms then provides the following:

$$-I_B(R_B + (\beta + 1)R_E) + V_{CC} - V_{BE} = 0$$

Multiplying through by (–1), we have

$$I_B(R_B + (\beta + 1)R_E) - V_{CC} + V_{BE} = 0$$

with

$$I_B(R_B + (\beta + 1)R_E) = V_{CC} - V_{BE}$$

and solving for I_B gives

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}} \tag{4.17}$$

Note that the only difference between this equation for I_B and that obtained for the fixed-bias configuration is the term $(\beta + 1)R_E$.

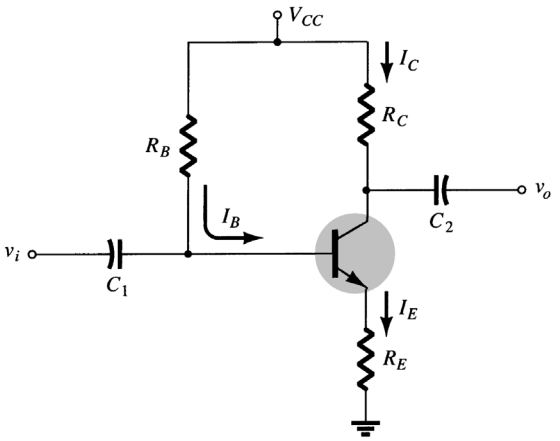

Fig. 4.17 BJT bias circuit with emitter resistor.

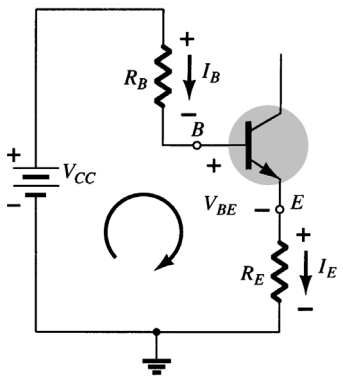

Fig. 4.18 Base-emitter loop.

There is an interesting result that can be derived from Eq. (4.17) if the equation is used to sketch a series network that would result in the same equation. Such is the case for the network of Fig. 4.19. Solving for the current I_B results in the same equation as obtained above. Note that aside from the base-to-emitter voltage V_{BE}, the resistor R_E is *reflected* back to the input base circuit by a factor $(\beta + 1)$. In other words, the emitter resistor, which is part of the collector-emitter loop, "appears as" $(\beta + 1)R_E$ in the base-emitter loop. Since β is typically 50 or more, the emitter resistor appears to be a great deal larger in the base circuit. In general, therefore, for the configuration of Fig. 4.20,

$$\boxed{R_i = (\beta + 1)R_E} \tag{4.18}$$

Equation (4.18) will prove useful in the analysis to follow. In fact, it provides a fairly easy way to remember Eq. (4.17). Using Ohm's law, we know that the current through a system is the voltage divided by the resistance of the circuit. For the base-emitter circuit the net voltage is $V_{CC} - V_{BE}$. The resistance levels are R_B plus R_E reflected by $(\beta + 1)$. The result is Eq. (4.17).

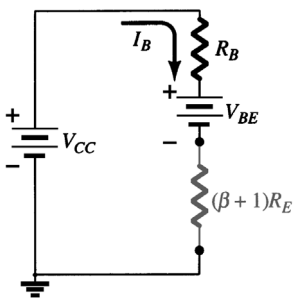

Fig. 4.19 Network derived from Eq. (4.17).

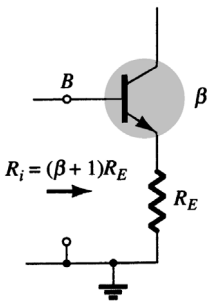

Fig. 4.20 Reflected impedance level of R_E.

Collector-Emitter Loop

The collector-emitter loop is redrawn in Fig. 4.21. Writing Kirchhoff's voltage law for the indicated loop in the clockwise direction results in

$$+I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

Substituting $I_E \cong I_C$ and grouping terms gives

$$V_{CE} - V_{CC} + I_C(R_C + R_E) = 0$$

and

$$\boxed{V_{CE} = V_{CC} - I_C(R_C + R_E)} \tag{4.19}$$

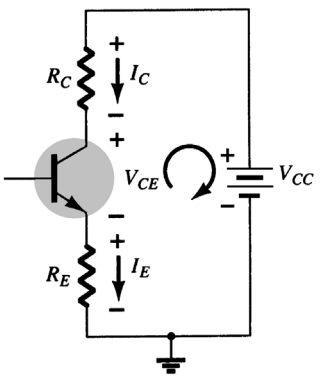

Fig. 4.21 Collector-emitter loop.

The single-subscript voltage V_E is the voltage from emitter to ground and is determined by

$$\boxed{V_E = I_E R_E} \tag{4.20}$$

whereas the voltage from collector to ground can be determined from

$$V_{CE} = V_C - V_E$$

and

$$\boxed{V_C = V_{CE} + V_E} \tag{4.21}$$

or

$$\boxed{V_C = V_{CC} - I_C R_C} \tag{4.22}$$

The voltage at the base with respect to ground can be determined from

$$\boxed{V_B = V_{CC} - I_B R_B} \tag{4.23}$$

or

$$\boxed{V_B = V_{BE} + V_E} \tag{4.24}$$

Example 4.4 For the emitter bias network of Fig. 4.22, determine:

a. I_B.

b. I_C.

c. V_{CE}.

d. V_C.
e. V_E.
f. V_B.
g. V_{BC}.

Solution:

a. Eq. (4.17): $$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20\text{ V} - 0.7\text{ V}}{430\text{ k}\Omega + (51)(1\text{ k}\Omega)}$$
$$= \frac{19.3\text{ V}}{481\text{ k}\Omega} = \mathbf{40.1\ \mu A}$$

b. $I_C = \beta I_B$
$= (50)(40.1\ \mu\text{A})$
$\cong \mathbf{2.01\text{ mA}}$

c. Eq. (4.19): $V_{CE} = V_{CC} - I_C(R_C + R_E)$
$= 20\text{ V} - (2.01\text{ mA})(2\text{ k}\Omega + 1\text{ k}\Omega) = 20\text{ V} - 6.03\text{ V}$
$= \mathbf{13.97\text{ V}}$

d. $V_C = V_{CC} - I_C R_C$
$= 20\text{ V} - (2.01\text{ mA})(2\text{ k}\Omega) = 20\text{ V} - 4.02\text{ V}$
$= \mathbf{15.98\text{ V}}$

e. $V_E = V_C - V_{CE}$
$= 15.98\text{ V} - 13.97\text{ V}$
$= \mathbf{2.01\text{ V}}$

or $V_E = I_E R_E \cong I_C R_E$
$= (2.01\text{ mA})(1\text{ k}\Omega)$
$= \mathbf{2.01\text{ V}}$

f. $V_B = V_{BE} + V_E$
$= 0.7\text{ V} + 2.01\text{ V}$
$= \mathbf{2.71\text{ V}}$

g. $V_{BC} = V_B - V_C$
$= 2.71\text{ V} - 15.98\text{ V}$
$= \mathbf{-13.27\text{ V}}$ (reverse-biased as required)

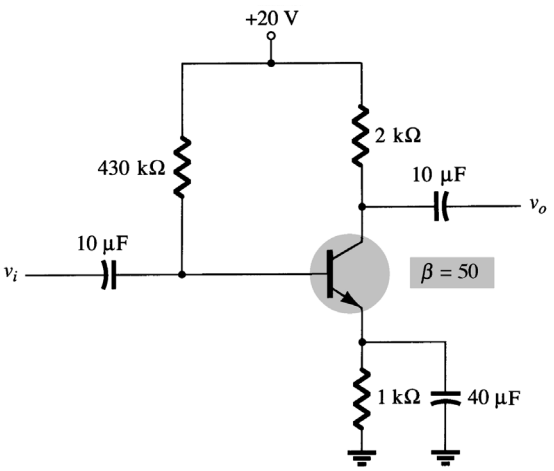

Fig. 4.22 Emitter-stabilized bias circuit for Example 4.4.

Improved Bias Stability

The addition of the emitter resistor to the dc bias of the BJT provides improved stability, that is, the dc bias currents and voltages remain closer to where they were set by the circuit when outside conditions, such as temperature and transistor beta, change. Although a mathematical analysis is provided in Section 4.10, some comparison of the improvement can be obtained as demonstrated by Example 4.5.

Example 4.5 Prepare a table and compare the bias voltage and currents of the circuits of Fig. 4.7 and Fig. 4.22 for the given value of $\beta = 50$ and for a new value of $\beta = 100$. Compare the changes in I_C and V_{CE} for the same increase in β.

Solution: Using the results calculated in Example 4.1 and then repeating for a value of $\beta = 100$ yields the following:

β	I_B (μA)	I_C (mA)	V_{CE} (V)
50	47.08	2.35	6.83
100	47.08	4.71	1.64

The BJT collector current is seen to change by 100% due to the 100% change in the value of β. The value of I_B is the same, and V_{CE} decreased by 76%.

Using the results calculated in Example 4.4 and then repeating for a value of $\beta = 100$, we have the following:

β	I_B (μA)	I_C (mA)	V_{CE} (V)
50	40.1	2.01	13.97
100	36.3	3.63	9.11

Now the BJT collector current increases by about 81% due to the 100% increase in β. Notice that I_B decreased, helping maintain the value of I_C — or at least reducing the overall change in I_C due to the change in β. The change in V_{CE} has dropped to about 35%. The network of Fig. 4.22 is therefore more stable than that of Fig. 4.7 for the same change in β.

Saturation Level

The collector saturation level or maximum collector current for an emitter-bias design can be determined using the same approach applied to the fixed-bias configuration: Apply a short circuit between the collector-emitter terminals as shown in Fig. 4.23 and calculate the resulting collector current. For Fig. 4.23

$$I_{C_{\text{sat}}} = \frac{V_{CC}}{R_C + R_E} \tag{4.25}$$

The addition of the emitter resistor reduces the collector saturation level below that obtained with a fixed-bias configuration using the same collector resistor.

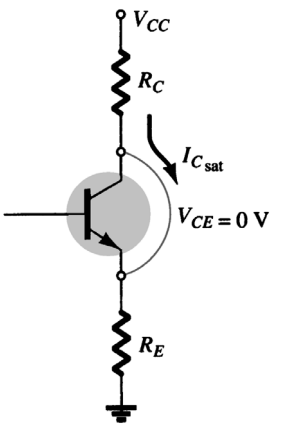

Fig. 4.23 Determining $I_{C_{sat}}$ for the emitterstabilized bias circuit.

Example 4.6 Determine the saturation current for the network of Example 4.4.

Solution:

$$I_{C_{\text{sat}}} = \frac{V_{CC}}{R_C + R_E}$$
$$= \frac{20\text{ V}}{2\text{ k}\Omega + 1\text{ k}\Omega} = \frac{20\text{ V}}{3\text{ k}\Omega}$$
$$= \mathbf{6.67\text{ mA}}$$

which is about three times the level of I_{C_Q} for Example 4.4.

Load-Line Analysis

The load-line analysis of the emitter-bias network is only slightly different from that encountered for the fixed-bias configuration. The level of I_B as determined by Eq. (4.17) defines the level of I_B on the characteristics of Fig. 4.24 (denoted I_{B_Q}).

The collector-emitter loop equation that defines the load line is

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

Choosing $I_C = 0$ mA gives

$$\boxed{V_{CE} = V_{CC}\big|_{I_C=0\text{ mA}}} \tag{4.26}$$

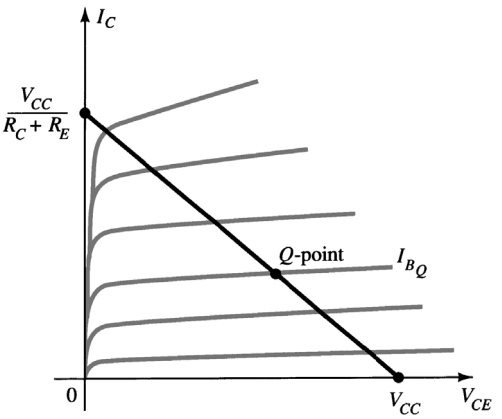

Fig. 4.24 Load line for the emitter-bias configuration.

as obtained for the fixed-bias configuration. Choosing $V_{CE} = 0$ V gives

$$\boxed{I_C = \frac{V_{CC}}{R_C + R_E}\bigg|_{V_{CE}=0\text{ V}}} \tag{4.27}$$

as shown in Fig. 4.24. Different levels of I_{B_Q} will, of course, move the Q-point up or down the load line.

4.5 Voltage-Divider Bias

In the previous bias configurations the bias current I_{C_Q} and voltage V_{CE_Q} were a function of the current gain β of the transistor. However, since β is temperature sensitive, especially for silicon transistors, and the actual value of beta is usually not well defined, it would be desirable to develop a bias circuit that is less dependent on, or in fact is independent of, the transistor beta. The voltage-divider bias configuration of Fig. 4.25 is such a network. If analyzed on an exact basis, the sensitivity to changes in beta is quite small. If the circuit parameters are properly chosen, the resulting levels of I_{C_Q} and V_{CE_Q} can be almost totally independent of beta. Recall from previous discussions that a Q-point is defined by a fixed level of I_{C_Q} and V_{CE_Q} as shown in Fig. 4.26. The level of I_{B_Q} will change with the change in beta, but the operating point on the characteristics defined by I_{C_Q} and V_{CE_Q} can remain fixed if the proper circuit parameters are employed.

As noted above, there are two methods that can be applied to analyze the voltage-divider configuration. The reason for the choice of names for this configuration will become obvious in the analysis to follow. The first to be demonstrated is the *exact method*, which can be applied to *any* voltage-divider configuration. The second is referred to as the *approximate method* and can be applied only if specific conditions are satisfied. The approximate approach permits a more direct analysis with a savings in time and energy. It is also particularly helpful in the design mode to be described in a later section. All in all, the approximate approach can be applied to the majority of situations and therefore should be examined with the same interest as the exact method.

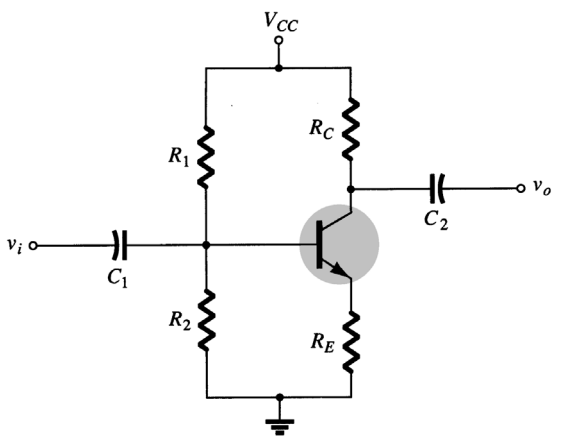

Fig. 4.25 Voltage-divider bias configuration.

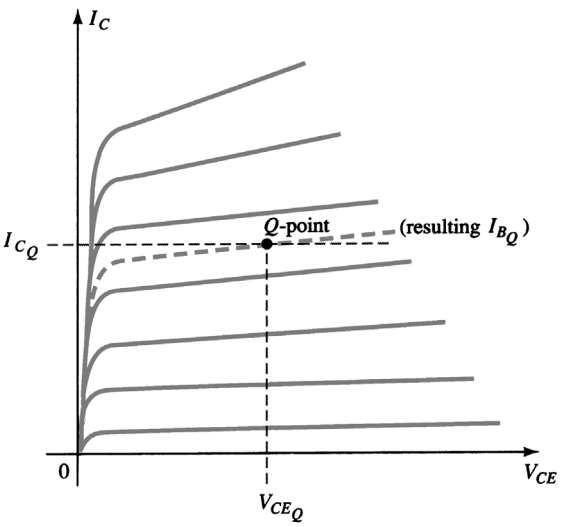

Fig. 4.26 Defining the *Q*-point for the voltage-divider bias configuration.

Exact Analysis

The input side of the network of Fig. 4.25 can be redrawn as shown in Fig. 4.27 for the dc analysis. The Thévenin equivalent network for the network to the left of the base terminal can then be found in the following manner:

***R*Th** The voltage source is replaced by a short-circuit equivalent as shown in Fig. 4.28:

$$R_{\text{Th}} = R_1 \| R_2 \tag{4.28}$$

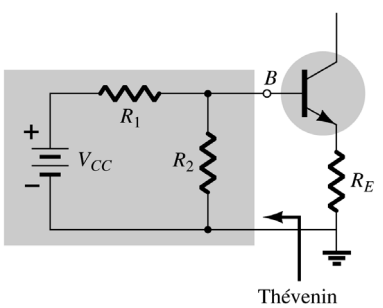

Fig. 4.27 Redrawing the input side of the network of Fig. 4.25.

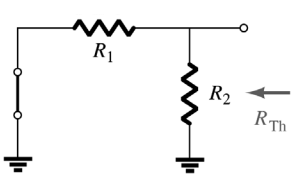

Fig. 4.28 Determining R_{Th}.

***E*Th** The voltage source V_{CC} is returned to the network and the open-circuit Thévenin voltage of Fig. 4.29 determined as follows:

Applying the voltage-divider rule gives

$$E_{\text{Th}} = V_{R_2} = \frac{R_2 V_{CC}}{R_1 + R_2} \tag{4.29}$$